AMENDMENTS TO THE SPECIFICATION

Paragraph at page 3, lines 16-27:

In Fig. 1, which is a plan view illustrating a prior art LCD apparatus, a gate bus line GL_i (i=1, 2, ..., m) and a signal bus lines SL_j (j=1, 2, ..., n) are provided on a transparent substrate [[17]] 11, and a pixel P_{ij} is provided at an intersection between the gate bus line GL_i and the signal bus line SL_j. Also, the pixel P_{ij} is constructed by a thin film transistor (TFT) Q, a liquid crystal cell LC and a storage capacitor SC. In this case, the liquid crystal cell LC is connected to a common electrode line [[CE_j]] CE_i arranged in parallel with the gate bus line GL_i. Also, the storage capacitor SC is connected to an adjacent gate line in a gate storage type or a storage line (not shown) in a storage capacitor type, thereby substantially increasing the capacitance of the liquid crystal cell LC.

Paragraph at page 4, lines 5-12:

In the LCD apparatus of [[Fig.]] Figs. 1 and 2, in order to easily specify a defective location, an address mark is provided for the gate bus line GLi and the common electrode line CE_i (i=1, 2, ..., m) as illustrated in Fig. 3 (see Fig. 3 of JP-A-2000-147549). For example, a scan address mark "617" is provided for the gate bus line GL_{617} and the common electrode line CE_{617}, and a scan address mark "618" is provided for the gate bus line GL_{618} and the common electrode line CE_{618}.

Paragraph at page 4, line 30 to page 5, line 1:

In Fig. 7, which illustrates a first embodiment of the LCD apparatus according to the present invention, an address mark ~~marks~~ provided for the gate bus line GL_i and the common electrode line CE_i(i=1, 2, ..., m) is connected to the common electrode line CE_i(i=1, 2, ..., m). For example, a scan address mark "617" is connected to the common electrode line CE_{617}, and a scan address mark "618" is connected to the common electrode line CE_{618}.